Title: Research Associate/Research Fellow for RF/mm-wave IC Design  
Location: VIRTUS, IC Design Centre of Excellence, School of EEE  
Positions: 5

Job Description:
We are actively seeking motivated and talented RF/mm-wave IC design engineers who want to join a dynamic and experienced team and take their technical knowledge to the next level. You will be responsible for the design of 60GHz radios using advanced process technology. Design of RF/mm-wave IC blocks such as low noise amplifiers, power amplifiers, mixers, front-end RF PLL and transceivers, RF synthesizers and IF filters will be based on 65nm RFCMOS process and/or 0.18um SiGe technology. You may help with transistor modeling for RF design, RF board and module design as well as lab test and characterization.

Requirements:
* MS (or higher) in Electrical Engineering with years of experience in analog and/or RFIC design (will also consider fresh PhD without any industry experience).
* Candidates must have design experience and knowledge in at least one of the following areas: RF blocks used in transmitter and receivers; RF front-end (LNA, mixers, PA drivers, RF-Filter, RF switches and VCO); PLL design
* Must have RF transistor level design skills.
* IC design experience for mass production is preferred
* Familiar with SiGe/CMOS process for RF/mm-wave applications is highly desirable.
* Must possess good communication skills.
* Must be self-starter, have passion in his/her work, and a good team player.

Interested candidates, please download application form from NTU website and email it together with his/her CV (in MS WORD) to H-EEE2@ntu.edu.sg

Professor YEO Kiat Seng,  
Interim Director, VIRTUS, IC Design Centre of Excellence  
School of EEE  
Email : H-EEE2@ntu.edu.sg
Title: Research Associate/Research Fellow for VLSI Design  
Location: VIRTUS, IC Design Centre of Excellence, School of EEE  
Positions: 3

Job Description:
We are actively seeking motivated and talented VLSI IC design engineers who want to join a dynamic and experienced team and take their technical knowledge to the next level. You will be responsible for the design of monitor and control circuits for 60GHz radios using leading edge process technology. Design of RTL with standard bus interface for System-on-Chip (SoC) low-power applications will be based on 65nm RFCMOS process and/or 0.18um SiGe technology. You may help with digital interface between RFIC and digital base band. You will need work with RFIC designers and board designers for RF design, RF board and module design as well as lab test and characterization in an embedded software environment.

Requirements:
* BS/MS/PhD in EE or equivalent with more than 5 years of working experience in RTL design of SoC products (e.g. in RF SoC).
* Excellent hand-on RTL design experience in synthesis, static timing closure, formal verification, gate level simulations & block level function verification.
* Good design knowledge in at least one of the industry standard bus interfaces (PCIe, SPI, SRIO, USB, XAUI etc) and memory interfaces (DDR2, DDR3 etc).
* Good experience in interfacing with architecture and physical implementation teams.
* Familiar with all aspects of chip development process with proficiency in front end design tools and methodologies.
* Experience in designing high speed/high performance SoC products is a plus.
* IP selection and interaction with 3rd party IP vendors with respect to front end design, timing views and associated integration is preferred.
* Coding experience in scripting languages such as PERL, TCL and UNIX shell etc.
* Familiar with foundry silicon operations and job views.
* IC design experience for mass production is preferred
* Must possess good communication skills.
* Must be self-starter, have passion in his/her work, and a good team player.

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Professor YEO Kiat Seng,  
Interim Director, VIRTUS, IC Design Centre of Excellence  
School of EEE  
Email : H-EEE2@ntu.edu.sg
Title: Research Associate/Research Fellow for Device Characterization and Modeling  
Location: VIRTUS, IC Design Centre of Excellence, School of EEE  
Positions: 2  

Job Description:  
Review and analyze foundry design rules and Foundry Design Kit (FDK) along with implementing FDK in a design simulation environment. Provide technical support/collaboration for/with IC designers. Work with IC/CAD teams to generate an advanced strategy to implement a design simulation environment for RF/analog/mm-wave/digital IC design in SiGe/CMOS technology. Design and layout test structures for device characterization/modeling and process control monitors. Test/measure system set-up for DC/CV/RF measurements for device modeling & characterization. Device characterization and modeling include, but not limited to test/measurement system calibration and RF de-embedding; data acquisition and selection (filtering) for device characterization & modeling; device model generation with process corner and statistical models as well as device layout/architecture optimization.  

Requirements:  
* MS (or higher) in Electrical Engineering with years of experience in device modeling implementation and verification skills (will also consider fresh PhD without any industry experience).  
* In-depth understanding on device physics of MOSFETs, BJTs, MOS/junction varactors, and passive devices (L, C, and R) in SiGe/CMOS technology.  
* Familiar with BSIM3/4, PSP, GP models and RF passive device models.  
* Process integration, design of test-chip and RF calibration structures experiences are preferred.  
* Some knowledge in IC packaging technology.  
* Experience in IV/CV/1-f/RF/temp characterization and modeling of semiconductor devices.  
* Familiar with IC-CAP and/or Cadence design tools (SpectreRF, Virtuoso, ADS etc).  
* MM-wave devices and circuits modeling is a plus.  
* Industry modeling experience for mass production is preferred.  
* Must possess good communication skills.  
* Must be self-starter, have passion in his/her work, and a good team player.  

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Professor YEO Kiat Seng,  
Interim Director, VIRTUS, IC Design Centre of Excellence  
School of EEE  
Email : H-EEE2@ntu.edu.sg
Title: Project Officer/Research Associate/Research Fellow for IC Packaging
Location: VIRTUS, IC Design Centre of Excellence, School of EEE
Positions: 2

Job Description:
You will support SoC/SiP based high speed digital, RF/analog/mm-wave and power management IC packages for wireless communication chipsets. Job responsibilities for this position include competitive analysis, technology road mapping and concept analysis for new IC package selection based on requirements for mechanical, thermal and electrical performance to achieve lowest system level cost. Perform high-speed design constraint management, design implementation, system co-design of IC-PKG-PCB and documentation of design specifications. S/He will work with marketing/IC/product teams on competitive analysis and road mapping package technology for future products.

Requirements:
* BS/MS/PhD in EE or equivalent with more than 3 years of working experience in IC package design technology and configurations including wire bond, flip-chip, SiP, PoP, PiP, stacked die, module and discrete.
* Familiar with IC package design flow methodology and implementing of high speed interface SI constrains for jitter, IR drop, cross-talk, and SSN specs.
* Experience in IC package level netlist capture, mechanical/electrical constraint management and package level thermal performance and enhancement techniques.
* System level co-design methodology of IC, package and PCB/board.
* IC top level floor planning including hard macro block placement, pad ring, RDL and bump pattern/assignment.
* IC package pinout optimization incorporating system level trade-offs of pad/bump assignment, package routing and PCB target component pinouts.
* Familiar with HFSS, IE3D, Sonnet, CST; PCB design and layout tools like PADs, Cadence; Downstream Tech CAM350; AutoCAD, Pro/E; Microsoft: Excel, Word, PowerPoint, Visio and MS Project; Operating Systems: UNIX/Linux and Windows.
* Industry IC packaging experience for mass production is preferred.
* Must possess good communication skills.
* Must be self-starter, have passion in his/her work, and a good team player.

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Professor YEO Kiat Seng,
Interim Director, VIRTUS, IC Design Centre of Excellence
School of EEE
Email : H-EEE2@ntu.edu.sg
Title: Research Associate/Research Fellow for Analog IC Design  
Location: VIRTUS, IC Design Centre of Excellence, School of EEE  
Positions: 5

Job Description:  
You will be responsible for the analog integrated circuit (IC) design in power management portion for System-on-Chip (SoC) of wireless front-end. Design work will include low voltage SiGe/CMOS circuit design and simulation as well as IC design layout, post-simulation and evaluation.

Requirements:  
* MS/PhD in EE or equivalent.  
* Preferably with at least 1 year working experience in CMOS/SiGe process.  
* Basic knowledge in the design of regulator, dc to dc/dc to ac/ac to dc converter.  
* Knowledge in the design of op-amp, bandgap, voltage reference and comparator and other analog building blocks.  
* At least one silicon approved IC experience.  
* Industry IC packaging experience for mass production is preferred.  
* Must possess good communication skills.  
* Must be self-starter, have passion in his/her work, and a good team player.

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Professor YEO Kiat Seng,  
Interim Director, VIRTUS, IC Design Centre of Excellence  
School of EEE  
Email: H-EEE2@ntu.edu.sg
Title: Project Officer/Research Associate/Research Fellow for RF/microwave Circuit Design
Location: VIRTUS, IC Design Centre of Excellence, School of EEE
Positions: 5

Job Description:
You will be responsible for the development of RF/microwave circuits and modules for ultra-wide bandwidth applications. S/He will also design, analyze, integrate and test RF hardware and its supply circuitry. Other responsibilities include board-level RF/analog design and design of RF and analog PWB/PCB.

Job Requirement:
* BS/MS/PhD in EE or equivalent.
* Preferably with at least 1 year working experience in CMOS/SiGe process.
* Strong experience in RF/microwave MIC circuits & modules design using EM, ADS and Cadence software.
* Hand-on experience in the measurement of RF/microwave circuits and modules using PNA, VNA, spectrum analyzer, noise analyzer etc.
* Strong R&D background in RF passive designs, such as RF Filters and coupler, is preferred.
* MMIC design experiences, like ultra-wide bandwidth LNA, PA, are preferred.
* Must possess good communication skills.
* Must be self-starter, have passion in his/her work, and a good team player.

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