Experienced Digital Design Engineer

The Team:
The team is responsible for the design and characterization of CMOS ASICs for thermal inkjet printheads.

The Job:
The job is primarily digital ASIC design and top-level circuit integration and may include efforts in one or more of the following areas:

• Investigation of customer needs and circuit solutions.
• Working with others to create a specification for the design.
• Digital design in both schematic capture (device level) and Verilog (RTL & structural).
• Integration of analog circuit blocks into top-level design.
• Synthesis & auto routing of standard cell blocks.
• Formal verification
• Overseeing physical implementation (layout).
• Vector creation using PERL and proprietary tools.
• Design verification through simulation and LVS compare.
• Timing closure through parasitic extraction, back-annotation & simulation
• Documentation of the design.
• Assisting with device characterization and debug.
• Assisting test engineering to create a production test program.
• New technology development: This work involves investigation work on new technologies. This may involve ASIC design, general circuit design, or blue sky investigation. This work can involve high level system architecture.

Requirements:
• Bachelor or Master degree in electrical engineering (IC design focus).
• Minimum of 3-5 years of experience doing ASIC design, including Verilog, simulation, physical layout, layout verification, and back-annotation. Completion of at least two full design cycles.
• Solid understanding of digital design fundamentals: CMOS fundamentals and combinational logic, sequential logic, multiplexer, flip-flop, counters, shift register, state machines etc.
• Basic understanding of mixed-signal circuits (op-amps, A/D’s, D/A’s, voltage references, etc.).
• Fluency with Linux.
• Fluency with Perl.
• Fluency with Verilog (RTL) and synthesis design flows.
• Fluency with place & route tools.
• Fluency with physical verification tools (layout vs. schematic, parasitic extract, back-annotation).
• Solid understanding of CMOS device structure and behavior.
• Solid understanding of power and clock routing/distribution.
• Solid understanding of SPICE and ability to model and simulate critical paths and power drops.
• Familiarity with production test equipment and methods so as to be able to support vectors, test development, and part debug.
• Candidates must have excellent organizational skills, good English oral and written communications skills, and a high level of interpersonal skills.
• Must be a self-motivated team player with the ability to work in a customer oriented, fast-paced, and demanding environment with minimal supervision.
• Leadership qualities: Integrity, attention to detail, timeline sensitive, goal oriented, and motivator.

Desired:
• Fluency in Python, Bash, TCL, C, JMP
• Familiarity with test data analysis in JMP
• Mentor-specific tool experience. Modelsim/Questa, Calibre, Pyxis Schematic, Eldo.
• Synopsys-specific tool experience: Astro router, Primetime, Design Compiler, TCAD sentaurus.
• Lint and formal verification tools (e.g. nlint, conformal, design compiler).
• Familiarity with layout tools (Pyxis Layout).
• Experience in analog design.
• Experience with mixed-signal design/simulation.
• Experience with oscilloscopes, and other electronic test equipment.

Contact:

Please email resumes to mun-hooi.yaow@hp.com. Only shortlisted candidates will be notified.

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