VIRTUS advances discovery and design (D&D) as well as research and development (R&D) in IC design and technology for applications in medical technology, clean technology and consumer electronics. Jointly funded by the Nanyang Technological University and Economic Development Board, the centre's research areas are mainly in analog, mixed-signal, power management and data converters, energy harvesting, low-power RF and mm-wave IC's, and new technology directions such as 3D-integration and physical design, 3D RF and mixed-signal circuits, and terahertz IC.

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Siek Liter received the B.A.Sc. from University of Ottawa (OU), the M.Eng.Sc. from University of NSW (UNSW); and the PhD from Nanyang Technological University (NTU) with over 30 years of experience from the industry and the university in Analog/Mixed Signal IC Design. He is currently the Director of VIRTUS, IC Design Centre of Excellence in the School of Electrical and Electronic Engineering in NTU as well as the Director for the Joint NTU-TUM PhD & MSc (IC Design) Programmes. His research interests are in the design of analog/mixed signal ICs especially in the areas of Power Management circuits, PLLs and ADCs.

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Yeo Kiat Seng is a widely known authority and world leader in the field of integrated circuit design. He has secured over S$30M of research funding, published 6 books, 5 book chapters, over 400 international top-tier refereed journal and conference papers and holds 35 patents. He gave keynotes/invited talks at international conferences, served in the editorial board of IEEE Transactions on Microwave Theory and Techniques and holds/held key positions as Advisor, General Chair, Co-General Chair and Technical Chair in international conferences. Dr. Yeo was awarded the Public Administration Medal (Bronze) on National Day 2009 by the President of the Republic of Singapore and was also awarded the distinguished Nanyang Alumni Award in 2009 for his outstanding contributions to the university and society.

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**Founding Director**

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28.8dBm, High Efficiency, Linear GaN Power Amplifier with In-Phase Power Combining for IEEE 802.11p Applications

In the near future, it is possible to implement electronic road pricing without having a physical toll gate and in-vehicle unit. Dedicated Short Range Communication (DSRC) based on IEEE 802.11p standard is an emerging technology for vehicular communications to implement such virtual toll system. To mitigate multipath and highly mobile channel environments between cars, IEEE 802.11p specifies a double guard interval and a half guard band along with higher output power when compared with the IEEE 802.11a standard, which results in a maximum 27Mbps data rate in 10MHz bandwidth at 5.85~5.925GHz carrier frequency band with 28.8dBm maximum output power.

Asst. Prof. Boon Chirn Chye and his team members Dr. Pilsoon Choi, Mao Mengda and Liu Hang have implemented and demonstrated a power amplifier (PA) for IEEE802.11p applications, adopting a new power combining technique in a 250nm GaN process. The proposed technique is used to improve the drain efficiency (DE) across the output power levels and meet the stringent error vector magnitude (EVM) requirement without any complicated input and output networks. Fig. 1 shows that the PA is implemented with a fabricated GaN die using the Chip-On-Board (COB) technology and tested with 27Mbps IEEE802.11p signal. It achieves -30.5dB EVM at 28.8 dBm output power, with a back-off DE of 22.4% at 30V supply at 5.72GHz without pre-distortion, as shown in Fig. 2. It also maintains more than 22% DE through supply voltage control while meeting its linearity requirement across the wide range of output power levels. The proposed circuit technique is viable for improving efficiency and optimizing linearity due to its simple architecture. This work was published in IEEE Microwave and Wireless Components Letters and a US patent has been filed.

A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer with In-Phase Injection-Coupled (IPIC) QVCO in 65 nm CMOS Technology

In order to achieve multi-gigahertz high-data-rate communication systems such as 60GHz band application, the requirements of PLLs keep getting higher. In an mm-wave direct-conversion transceiver, the generation of quadrature local oscillator (LO) signals is challenging. The conventional techniques to generate quadrature LO signals suffer from many problems. The method of using divide-by-2 divider after a voltage-controlled oscillator (VCO) with double LO frequency is popular in multi-GHz designs, but it is difficult to be realized in mm-wave frequency. Employing passive RC complex filter is another way to generate quadrature signals, but to compensate its loss requires high power in mm-wave frequency. The conventional parallel-coupled QVCO seems to be a good choice for mm-wave application. Asst. Prof. Boon Chirn Chye and his team members Yi Xiang, Liu Hang and Lin Jiafu have implemented and demonstrated a low power fully integrated 60 GHz quadrature PLL. As shown in Fig. 3, through a particular symmetrical coupling network, the in-phase coupling is realized in the proposed IPIC-
Linear Angle Sensitive Pixels for 4D Light Field Capture

Light at a given point in space can be represented by an infinite collection of rays from all other points in space. This infinite collection of rays can be treated as a vector field, called the light field. The mathematical formulation of light field consists of a 7 dimensional function is called the plenoptic function. The function describes the light intensity at any point in space, at all times, for all wavelengths (color) and from all viewing directions. It comprises the intensity along the two spatial directions x and y, along with the wavelength (\(\lambda\)), time (t) and the three viewing directions (Vx, Vy and Vz). Since it is impractical to sample this 5D function which deals with \(P(x, y, Vx, Vy, Vz)\), a reduced 4D representation has been developed and used extensively. This 4D representation provides a more complete description of the visual scene around us. Conventional image sensors can only capture a 2D version of the image scene and hence provide limited capabilities for post capture image enhancement. The complete 4D information allows for faithful 3D reconstruction, post capture refocus and reconstruction of partly occluded objects. Integral photography was perhaps the first method proposed to recreate a 4D light field using the direction of incoming light rays. Since then many alternative techniques have been proposed for capturing the light angle information. Well known among them are the multi-aperture-based and the Talbot effect-based techniques. Multi-aperture-based techniques use an array of micro-lenses below the objective lens to capture the angle information. They require complex post processing and are computationally very intensive. On the other hand, Talbot effect-based techniques use on-chip diffraction gratings and have been touted as a suitable alternative for light angle capture. This technique takes advantage of the microscale Talbot effect and encodes angle information in terms of intensity. However, the response produced by pixels employing this technique is cosine in nature and a large number of pixels are required to faithfully estimate the angle information.

Asst. Prof. Chen Shoushun’s team designed a new pixel structure capable of detecting light angles along both the horizontal and vertical directions. The number of sub-pixels to distinctly determine the angles are very low (4 pixels) compared to the Talbot effect-based technique (8 pixels for both directions). The response is linear and is independent of the incident wavelength.

A proof-of-concept sensor was fabricated in 65 nm Global Foundries mixed-signal process. The pixel array is made up of 12 x 10 macro pixel clusters. The proposed structure can distinguish between angles over a broad range of 70°: from -35° to +35°. The sensitivity of response can be increased by using a higher metal layer compared to the one used in this design (metal 5). As a result of this new passive angle detection technique, Asst. Prof. Chen and his team expect further advancement in the field of 3D image capture and object recognition.
An Adaptive Integration Time CMOS Image Sensor for Star-Tracker Application

Recent years have witnessed a trend in space technology that highlights the importance of mini and micro satellite missions. Earth-observation satellites need automatic attitude control system to steer the satellite to the desired observation point. Therefore many satellites are equipped with various navigation sensors (Earth magnetic, gyros, Sun sensor and star tracker) and observation sensors (imaging camera). Among these sensors, star trackers are the most accurate solution with a bore sight accuracy in the range of arcseconds. Star radiation is measured by its visual magnitude. A star with Apparent Magnitude $M_V = 2.5$ times brighter than a magnitude $M_V = 2$ star. Using the Sun as reference, which has an Apparent Magnitude of $M_V = -26.76$ and solar flux of 1.3 kW/m², we can easily derive any other star's luminance. By taking into factors such as luminance spectral distribution, photo detector's quantum efficiency (QE) and lens point spread function (PSF), we can estimate the number of generated photons received by the camera. For a star tracker with 3 cm lens aperture, 85% lens transmission efficiency, 1 pixel PSF, and 200 ms exposure time, a star with $M_V = 6$ can generate 1195 photons at the center pixel of the star. In order to achieve higher altitude accuracy, it is preferable to shorten the exposure time. In the above calculation, 200 ms produces a systematic error of 48 arc-second for an orbital period of 90 minutes. With a shorter exposure time, say 50 ms, the number of photons at the center pixel of the same star will drop to only 298. This is a very challenging number for CMOS image sensor, and in particular, under space radiation environment.

Asst. Prof. Chen Shoushun and his team have designed a novel CMOS image sensor architecture for star tracker application that allows adaptive integration time. Brighter pixels will be detected and read out at an earlier time to avoid saturation and dimmer pixels can have longer integration time. Due to the voltage detection nature of the sensor architecture, it can be categorized into the saturation detection scheme. Compared with other solutions in this category, the pixel maintains compact footprint and high fill factor. The shrinking size of the pixels can be beneficial to high-resolution integration to increase the field of view in star tracker. A proof-of-concept chip has been fabricated in Global Foundries 0.18μm 1P6M CMOS technology. The result shows that the architecture demonstrates a great potential for star tracker applications where pixel intensities are sparsely distributed.

Nano-Electro-Mechanical Non-Volatile Memory Design

Over the last few decades, power, performance, and capacity of embedded memories have constantly benefited from the scaling of CMOS technology. However, lower threshold voltage and smaller device channel length in scaled CMOS devices have led to an exponential increment in the leakage current ($I_{off}$). As a result, designing mainstream memories such as SRAM, DRAM or Flash in nano-scale technology is facing critical issues such as tight requirements on leakage and degraded immunity to process variations. Recent publications have reported several emerging technologies for achieving zero standby leakage in memory design. These include resistive RAM (R-RAM), magnetic RAM (M-RAM), phase-change RAM (PC-RAM), conductive-bridge RAM (CB-RAM), and ferroelectric-RAM (Fe-RAM). In these devices, different physical mechanisms (FLASH: floating gate, M-RAM: free magnetic layer, and Fe-RAM: ferroelectric polarization) are exploited to store data without power supply. However, they also fail to offer a good data retention at extreme temperature such as 200°C and above like mainstream technologies. NEMS-based memory devices utilize electrostatic force to perform set/reset operation and adhesion force between two smooth metal surfaces to retain data. It has been shown that metal-metal adhesion improves at higher temperature. This is because metal soften as temperature increases. As a result, NEMS-based memory devices can potentially offer seamless operation over a wide range of temperature.
temperature range for industrial or defense electronic applications. However, conventional NEMS-based NVM needs two separate actuation electrodes to perform the reset and write “1” operations.

This collaborative research, between Asst. Prof. Kim Tae Hyoung Tony and A*STAR IME, proposes a cantilever-based memory structure for storing binary data at extreme operating temperature (up to 300°C) in rugged electronics. The memory bit (0/1) is formed by opening/closing of an electrostatic switch. Permanent retention is obtained by adhesive force between two smooth surfaces in contact, eliminating leakage observed in all types of storage-layer-based NVMs. The Reset utilizes a train of short pulses to break the adhesion between the electrodes. This allows the Nano-Electromechanical Switch (NEMS) memory to be implemented using a simple bi-layer design and easily integrated with CMOS platforms. The investigators propose an array structure where each memory cell consists of a NEMS memory device and one NMOS transistor for full random-access operation. This research work was presented at IEEE European Solid-State Device Research Conference (ESSDERC2013).

**Design of High Sensitivity CMOS Sub-THz Imaging Receiver**

THz radiation (0.1~10 THz) has introduced new imaging approaches for biomedical and security diagnosis, with high sensitivity and no harmful ionization. A CMOS-based imager can further improve system integration with low cost. The primary challenge of CMOS mm-wave imager is the design of a high-sensitivity receiver that can compensate losses from both path propagation and also absorption of object under test. In addition, since a large imager array is required for high resolution, pixel size must be small. Super-regenerative receivers hold promise over conventional passive imaging receiver due to higher sensitivity by quench-controlled oscillators that enable oscillation-magnitude amplification of input RF signal within a narrow band. One 135GHz CMOS super-regenerative mm-Wave receiver is demonstrated

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**Fig. 10** SEM images of the fabricated cantilever-based NEM NVM devices

**Fig. 11** The proposed Sub-THz CMOS imaging system at 140GHz and 280GHz
Design of Dual-Mode CMOS ISFET Sensor for High-Throughput pH Detection

Unlike traditional ion-sensitive field-effect transistor (ISFET) devices that require ion-sensitive membrane by expensive post-processing, ISFET devices in standard CMOS process have drawn much attention recently by utilizing the top most passivation layer ($\text{Si}_3\text{N}_4$) for ion sensing. One emerging application is to detect the hybridization process of complimentary stranded DNA. Since protons ($\text{H}^+$) are released in this process, the pH of solution has correlated change in reaction chamber. However, unresolved challenges still exist for high-throughput pH detection. Firstly, it needs to locate one slice of DNA at precise spatial position and to generate local pH response at that position with accurate data correlation. Furthermore, the pixel-to-pixel mismatch needs to be reduced for large array readout with high accuracy.

To solve these problems, Asst. Prof. Yu Hao and his group members have designed a 64×64 1200fps dual-mode CMOS ISFET sensor fabricated in standard 0.18μm CMOS image sensor (CIS) process. Each ISFET pixel contains a dual-mode sensing region with active amplification. Dual-mode includes image mode and chemical mode. When one slice of DNA is attached to a micro-bead inside region of one ISFET pixel, its spatial location is identified during image mode via contact imaging. With the position of micro-bead determined, its local pH response can be measured during the chemical mode. In addition, correlated-double-sampling (CDS) is deployed to reduce pixel-to-pixel mismatch. The measurement results have successfully verified the state-of-the-art performance of the proposed dual-mode CMOS ISFET sensor for pH detection in portable and label-free DNA sequencing application. The pixel-to-pixel mismatch is reduced by correlated-double-sampling readout with FPN reduction from 4% to 0.3%. And the sensitivity reaches 103.8mV/pH. This work has been accepted for presentation at the ISSCC 2014 Student Research Preview.
Low Power Radar SOC

Current radar systems consume high power because Direct Digital Frequency Synthesizer (DDFS)-based chirp synthesizer (1-10 watts). It is heavy and bulky due to the use of discrete components and complex thermal management in it. Existing synthetic aperture radar (SAR) imaging systems are generally too heavy for small platforms, or too expensive in day-to-day use to be applied in small-scale civil applications. This research focuses on developing a multiple input multiple output (MIMO) dual band SAR system for Unmanned Aerial Vehicle (UAV) and/or inverse synthetic aperture radar (ISAR) imaging applications with integrated circuit solution. The proposed SAR system is compact (integration on single chip with size of 4 mm² except power amplifier and antenna), low power (<20 mW for transmitter and <50 mW for receiver) due to the innovative digital PLL-based chirp synthesizer design. The proposed RF system can achieve <15 cm resolution which is state of art. Besides, it can be operated on small UAV due to its low power and compact design. The developed system can also be applied in emerging smaller scale applications such as tracking of vehicles and localization of targets, real time surveillance, civil crisis. Funded by Defence Research Technologies Singapore (DRTECH), Asst. Prof. Zheng Yuanjin and his team members have been working on the development of a X/Ku band SAR sensor for UAVs with integrated circuit solution. Shown in the accompanying figure is the concept of miniaturizing radar sensors with integrated circuit solutions which reduce the system size and power consumption. The circuit blocks including frequency synthesizer, transmitter and receiver have been developed and are also shown as well as some test results. The frequency synthesizer is able to synthesize Linear Frequency Modulation (LFM) waveform with rms frequency error of less than 200 KHz. The integrated transmitter is able to transmit sufficient power of 10 dBm with small amplitude ripple. The receiver is able to perform stretch processing in which each single target return is compressed into a spectrum peak. The developed radar RF hardware will be loaded onto a UAV for field trial at the end of the project.
Research Statistics

CATEGORIES OF RESEARCH FUNDING (APPROVED IN 2013)

Defence $17,758,162.50 35.77%
Govt Agencies $11,699,439 23.57%
NTU $5,826,749 11.74%
A-Star $4,828,753.44 9.73%
Others* $3,849,438.84 7.75%
MOE $2,730,029 5.50%
Industry $1,758,380.24 3.54%
NRF $1,193,111 2.40%

TOTAL $49,644,063.02

FUNDING BY RESEARCH CENTRES (APPROVED IN 2013)

INFINITUS $5,695,678.50 11.47%
NOVITAS $8,871,233.44 17.87%
VALENS $1,655,353.80 3.33%
OPTIMUS $3,563,773.84 7.18%
LUMINOUS $0 0.00%
VIRTUS $7,597,937.44 15.30%
EXQUISITUS $5,630,104 11.34%
EMERL $7,352,15 1.48%
SaRC $13,947,000 28.09%
OTHERS** $1,947,767 3.92%

TOTAL $49,644,063.02

*Others include medical institutions, foreign funding agencies, institutes of higher learning and research institutes.
**Others include ER@N, TL@NTU and NTU (Provost’s/ President’s Office).

APPROVED RESEARCH FUNDING (NON-CUMULATIVE) S$MILLION

2009 2010 2011 2012 2013
60.99 36.36 45.46 43.82 5.83
17.42 7.2 4.68 22.98

Externally Funded Projects
Internally Funded Projects