INTRODUCTION

The year 2009 is another fruitful year for the division. It begins with the exciting news of a research breakthrough by a team of researchers in the division and Rice University. The project was led by Professor Krishna Palem, Kenneth and Audrey Kennedy Professor of Computing at the Department of Computer Science at the George Brown School of Engineering at Rice University and Professor Yeo Kiat Seng, Head of Division of Circuits and Systems and Interim Director of the new Integrated Circuit Design Centre of Excellence at NTU, with team members Associate Professor Goh Wang Ling and Visiting Assistant Professor Kong Zhi Hui. They have successfully developed a new super environmentally-friendly green chip which uses thirty times less energy while running seven times faster than existing chips. The year also ends with the establishment of a $50 million new Integrated Circuit Design Centre of Excellence jointly funded by EDB and NTU. This new centre will provide an excellent learning and research environment to train more than 100 integrated circuit (IC) designers and researchers to propel the knowledge based sector in Singapore.

To scale greater heights in IC research, the division has been actively looking for talented young researchers worldwide to join the division. Dr Zheng Yuanjin, a group leader in RFIC from the Institute of Microelectronics; Dr Chen Shoushun, a post-doc working in biosensor IC from Yale University; Dr Yu Hao, a senior research staff specializing in VLSI from Berkeley Design Automation; and Dr Tony Tae Hyoung Kim, a post-doc working in low-power memory circuit design from University of Minnesota, have joined the division as Assistant Professors. They add both depth and diversity in IC research activities in the division and help to position NTU to become one of the leading universities in the world for IC design research.

One of the new faculties, Dr Chen, has successfully tested and characterized a low power wireless motion sensor. The sensor features a 64 by 64 pixel array and can report standard analog intensity images. An ultra-wide-band (UWB) radio channel allows it to transmit digital temporal difference images wirelessly to a receiver with high rates and reduced power consumption. The sensor wakes up when it detects enough scene changes and only communicates meaningful frames. Hence, the power consumptions for the sensor and the radio transmission are 0.9 mW and 15 mW, respectively.
devices based on locally-accessible low temperature co-fired ceramic (LTCC) technology for emerging low-power high-speed wireless personal area network applications in the unlicensed millimeter-wave 60-GHz band.

Another project, “Batteryless Flexible Transceiver for Biomedical Applications” led by Professor Boon Chirn Chye, has secured $765,000 from MOE under the competitive AcRF Tier 2 Grant Call. The project aims to achieve our vision of the future wireless communications, all RF transceiver application devices (hand-phones, wireless identity card/cash cards, etc.) and wireless biomedical sensors are ultra-miniature and wearable-like accessories. In addition, they must have low heat dissipation and low interference to the extent that they could be used for biomedical applications without causing any hazard.

As part of the on-going effort to promote the exchanges of research ideas in IC design, an international symposium on integrated circuits (ISIC-2009) was jointly organized by the division and IEEE Singapore Section. The conference was supported by the IEEE Solid-State Circuits Society Singapore Chapter, Singapore Exhibition & Convention Bureau and M.I.D.A.S. The symposium has received more 200 papers. The accepted papers are presented in 14 Special Sessions, 16 Regular Oral Sessions, and 2 Poster Sessions. The Symposium invites two distinguished experts to deliver the keynotes - Dr. Bram Nauta from the University of Twente, the Netherlands and Mr. Frank P. Averdung, Chief Executive Officer, SUSS MicroTec AG, Germany. Dr. Bram Nauta and Mr. Frank P. Averdung will speak on Analog and RF Circuits in Nanometer CMOS and More than Moore - The Challenges of 3-Dimensional IC Integration, respectively. In addition, one tutorial on IC Design of Power Management Circuits is to be conducted by Professor Ki Wing-Hung from the Department of Electronic & Computer Engineering, The Hong Kong University of Science and Technology.

Fig. 2 Applications of battery-free flexible transceiver
The programme aims to draw different expertise of the members in the analog/mixed-signal IC design group that makes advances in the design of power aware mixed-signal system (PAMS). With the emerging of advanced CMOS process and technology together with traditional or new applications in integrated circuits for use in consumer, nanotechnology, biomedical, environmental and health care, the PAMS becomes an important programme platform that supports the urgent needs and design challenges.
Input Interface – A/P Chan Pak Kwong (Group Representative)
The design challenge of an input interface is to ensure sufficient quality of input signal amplification under low power design. For a sensor interface example, the objectives are to translate the minute sensing signal to an electrical form, amplify the signal with sufficient sensitivity with respect to noise and offsets, consume low power whilst preserving adequate dynamic range. One design example is the Electrical Capacitance Tomography (ECT) Imaging Transducer IC. Besides low power consumption, the precision design technique offers sub-fF detection in tolerant to wiring parasitic capacitances up to 150pF.

Analog and Digital Signal Processing – Asst/P Zheng Yuanjin
In this programme, the objective is to develop a system on chip (SoC) or system in package (SiP) device for wearable Wireless Body Area Networks (WBANs) for biosensing applications. The device integrates analog and digital building blocks to build a self-functional low power integrated circuit platform. In this work, a digital PHY baseband transceiver IC is proposed and implemented as a core module to enable a WBAN radio. The proposed transceiver is targeted at low data rate, ultra low power to sustain long battery life (2-3 years). Implemented in a 0.18-µm CMOS technology, the baseband chip consumes 240.24 µW for TX mode and 202.34 µW for RX mode when working at a 250 kHz system clock and 1.8V supply.

Data Converters – A/P Siek Liter
Data Converters as in Analog-to-Digital converters and Digital-to-Analog Converters are found before and after the digital signal processing block. One example of such a converter is the Dynamic Reference ADC. It consists of the same number of comparators as the number of output bits and each of the comparator’s voltage reference is dynamically controlled by its preceding bit stage in accordance with the input signal magnitude, as this converter computes in a serial manner. As such the Dynamic Reference ADC can be easily synchronized with its adjacent blocks using the timing clock of the peripheral blocks adjacent to it.
Low Power Digital Processor
– A/P Joseph Chang and A/P Gwee Bah Hwee
This project is part of the NTU - Linköping University research collaboration on advanced Asynchronous Logic Circuit Design. The IC chip was fabricated using the IBM 130 nm CMOS process comprising regular-Vt and low-power-Vt standard library cells. A comparison of the performance of the two Data Arithmetic Logic Units (DALUs) for 24-bit 56002 DSP shows that the power dissipation of the asynchronous design is superior (> 40% improvement) and the speed comparable or less than the former, depending on the algorithm.

Power Management System
– Asst/P Tan Meng Tong and Asst/P Zheng Yuanjin
The power management system provides regulated voltage to each of the sub-systems in the mixed-signal SOC system. To reduce the power consumption in power management system (PMS), the supply voltage of the digital processor will be made adjustable by a programmable digital DC-DC converter. The voltage will be adjusted according to the computation requirement of the digital processor. For example, when the digital processor is in the idle state, the supply voltage will be reduced to near subthreshold level. Otherwise, the supply voltage will be increased to the nominal level for computationally intensive operation.
The research activities of the RF Integrated Circuits and Systems Programme cover the following topics: Ultra Low Power Low Voltage RFIC Design; RF Frequency Synthesis, Modelling of Nano-meter Devices, Interconnects and Coupling of RFICs; EMC/EMI for RFICs; Packaging for RFICs, Antenna in Package and Antenna on Chip; RFIC Testing, and EDA Tools for RFIC. Most projects explore novel designs and analysis of devices, circuits, sub-systems and RF SoC (System on Chip) products. The main focuses are design challenges in high frequency, broad-band, low power performance, and flexibility & reconfigurability of the RF circuits and systems. The ultimate achievement will be the flexible RF front-ends and ultra low power circuits and systems which can be powered by alternative energy harvesting storage devices such as kinetic, electromagnetic and solar cells for certain biomedical applications. With the push for green electronics, research in energy harvesting storage devices and circuits is expected to become an important activity of the Programme. Some of the latest projects and significant achievements in 2009 are described under this programme as follows.

A Wideband Low-Power Low-Noise Amplifier in CMOS Technology

A T-coil network can be implemented as a high order filter for bandwidth extension. This technique is incorporated into the design of the input matching and output peaking networks of a low-noise amplifier. The intrinsic capacitances from the transistors are employed as part of the wideband structure to extend the bandwidth. Using the proposed topology, a wideband low-noise amplifier with a bandwidth of 3-8 GHz, a maximum gain of 16.4 dB and noise figure of 2.9 dB (min) is achieved. The total power consumption of the wideband low-noise amplifier from a 1.8 V power supply is 3.9 mW. The prototype is fabricated in 0.18 µm CMOS technology. This work will be published in IEEE TCAS-I on April. 2010.
Energy Aware RF Receiver Front-End for Low-Power 2.4-GHz Applications

In the interests of longer battery life, ultra-low power design has recently become a topic of intense interest for applications such as wireless personal area networks (WPAN), and wireless sensor nodes. The IEEE 802.15.4 standard has been specifically designed to cater to such applications. Transceivers which follow this standard have been designed to operate using less than 10 mA of DC current. These designs have relied on simplified circuit configurations to minimize power consumption. Despite their relative successes, we believe that significantly more power consumption can be saved both by further simplifying the circuit structures, and dynamically adjusting the performance of the receiver (RX). The latter method is termed energy-aware design.

While a radio is designed around its sensitivity, it normally operates under significantly better conditions. The average path loss varies depending on the environment, availability of line of sight (LOS) and distance between the RX and transmitter (TX), among other things. An energy-aware transceiver adjusts its performance according to the amount of received signal strength and uses the optimum power to receive the signal in a given situation. This work presents the implementation of an energy-aware RX front end for low power, low data-rate applications. We propose to dynamically control the power consumption of an RX front end based on the real-time required noise figure (NF). In order to limit the scope of our work, we will design around the IEEE 802.15.4 standard which operates in the 2.4-GHz Industrial, Scientific and Medical (ISM) band. We focus on the design of the RX front end which generally consumes a large portion of the total RX power. The standard features relaxed requirements in terms of interference rejection, and noise performance which simplifies front end design and will allow us to implement dynamic power control circuitry. A receiver front end designed in 0.18-µm CMOS consisting of an LNA and IQ mixers has been designed. The front end’s power consumption is controllable from 5.0 mA down to 1.4 mA. It is proposed to control the front end’s power consumption based on the real-time required noise performance. We show that under typical channel conditions, this front end can save up to 40% of its nominal power consumption. Figure 10 shows the micrograph of the fabricated design implemented in a 0.18 µm CMOS process.

![Fig. 10: Micrograph of a CMOS energy-aware receiver](image-url)
The research projects in VLSI Design group cover a broad spectrum of emerging and multi-disciplinary topics from low power and fault tolerance arithmetic circuits, subthreshold and current mode circuits for artificial neural network, biologically inspired imaging system, multi-voltage multi-frequency high level synthesis, memetic computing with evolvable hardware systems, dynamic energy and reliability management for multi-processor system-on-chip (SoC) architectures, 3D Network-on-Chip (NoC), design methodologies of low-complexity fixed and reconfigurable FIR filters, publicly authenticable watermarking for VLSI intellectual property protection to interconnect reliability analysis. The following research projects are highlighted in this report.

Three-dimensional Many-core Integrated System

New multimedia applications such as surgical simulation, visual reality visualization, city security surveillance require real-time processing of a large-volume of data. The new requirements for the design of high-performance VLSI systems, with heterogeneous functionary component, concurrent data processing and self-adaptive configuration, are beyond the scope of the conventional 2D integration due to interconnect limitation. 3D integration reduces the system size dramatically by vertically connecting multiple device layers by either wire-bonding or through-silicon via (TSV). The use of ‘device-stacking’ allows heterogeneous components fabricated from imager process, MEMS process, RF process, and logic process to be independently optimized and integrated together with a low fabrication-cost yet a high yield-rate. As there is a significant boost in the communication bandwidth, the 3D integration is suited for I/O-centric system with the concurrent real-time data processing. At the physical-level, as the many-core system consumes more power with more integrated components, the power supply and heat removal problems are challenged. Collaboration with Intel circuit lab at Oregon USA showed that TSVs are critical components for power and temperature integrity. With a compact and parametric physical model to abstract the complicated 3D system, a TSV design tool was developed to optimize the power and thermal integrity simultaneously. At the system-level, a real-time adaptive many-core system configuration and task distribution methodology is being developed to optimally distribute the computation and communication tasks onto the 3D many-cores under the bandwidth, temperature and power constraints. At the application-level, a currency discovering algorithm under the frame-work of synchronous data flow graph will be developed to optimally map the stream multimedia application into a task set with the maximum utilization of parallelism.

Fig. 11 (a) A physical-level view of 3D system with through-silicon via (TSV) for both power supply and heat-removal

(b) A system-level view of 3D system with many-cores, NoC bus and memory
Dynamic Energy/Reliability Management for Multi-Processor System-on-Chip (MPSoC)
Application-specific multi-core architectures with 8/16/32 or more homogeneous/heterogeneous CPU cores integrated on a single chip are the dominant trend for advanced processor architectures. From the technology integration perspective, it is relatively well understood how to build VLSI devices consisting of so many diverse building blocks. However, a key challenge for the feasibility of today and future many core Multi-Procoessor System-on-Chip (MPSoC) architectures is power dissipation density and energy consumption, which directly affects the robustness and reliability of the device operation. The VLSI research group has recently started a joint PhD research program with Technological University of Munich. The goal of this research is to investigate strategies and techniques to dynamically manage processor energy consumption in dependency to workload and environmental operating conditions. In general, processor resources are dimensioned for worst case workload requirements. However, worst case workload conditions typically apply only temporarily, not in sustained, long-term fashion. Hence, during normal or relaxed workload situations, processing resources can either be switched off or put into hot/cold stand-by in order to consume little or no energy. Existing techniques for energy management used in high-end mainframe computers will be effectively scaled down to chip-level multi-processors to optimize the trade-off between processing performance, power dissipation and device reliability.

Statistical Modeling of Electromigration Failures
In device reliability study, as there can be multiple failure modes in today ultra-large scale integration, it becomes imperative to identify the failure units with different failures before failure analysis in order to save time and also have an accurate assessment of reliability. A novel approach to statistical modeling of electromigration failure based on mixture distribution probability density function has been formulated, with the statistical observation confirmed by physical analysis using high-resolution electron microscope.

**Fig. 12** Mixture distribution probability density function

**Fig. 13** Physical analysis using high-resolution scanning electron microscope to confirm the statistical observation.
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PhD and MEng DEGREES AWARDED IN 2009

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MEng – Circuits & Systems

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<td>Design of Low-power High Speed Error-tolerant Adder and its Application in Digital Signal Processing</td>
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SELECTED PUBLICATIONS IN 2009

### SELECTED PUBLICATIONS IN 2009


